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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/828,516	04/19/2004	Matti Floman	915-007.087	4302

4955 7590 12/28/2006

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EXAMINER	
CAMPOS, YAIMA	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	12/28/2006	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/828,516	FLOMAN ET AL.	
	Examiner	Art Unit	
	Yaima Campos	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *24-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

RESPONSE TO AMENDMENT

1. The examiner acknowledges the applicant's submission of the amendment dated October 16, 2006. Claims 1-23 have been cancelled and claims 24-46 have been added. There are 23 claims pending in the application; there are 4 independent claims and 19 dependent claims, all of which are ready for examination by the examiner.

I. OBJECTIONS TO THE SPECIFICATION

2. **Claims 24, 35 and 42** is objected to because of the following informalities:

3. Claims 24, 35 and 42 recite the limitation "provides" in (Claim 24, line 11; Claim 35, line 3; Claim 42, line 10). It is believed this limitation contains a typographical error and should read **–provide-**.

4. Appropriate correction is required.

II. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. **Claims 24, 28-43 and 45** are rejected under 35 U.S.C. 102(b) as being anticipated by Camacho et al. (US 6,167,487).

7. As per **claims 24, 41-42 and 45** (new), Camacho discloses a memory unit comprising:

"a first processor in communication with a memory unit, and a second processor in communication with the memory unit" **["multi-port RAM that allows read and write accesses from different ports to be performed simultaneously" (Col. 1, lines 54-56)]**

at least two memory areas for storing data, **["a cache SRAM memory and a main DRAM memory arranged on the chip" (Col. 2, lines 10-19; Figure 1 and related text)]**

first terminals for accessing data within the memory areas, second terminals for accessing data within the memory areas, and **["single chip having first and second input/output pins" (Col. 2, lines 10-19; 28-45) "ports A and B" (Figure 1 and relate text)]**

at least two access controllers for selectively providing **["the first data path may be controlled independently of the second data path" (Col. 2, lines 20-22) "port A control 22" and "port B control 24" (Figure 1 and related text)]**

sole addressing and accessing data through one of the terminals, or **["the first and second data path may be arranged so as to provide a single port for input/output of a data combination to or from the cache memory" (Col. 2, lines 46-52)]**

individual addressing and accessing data through each of the terminals, respectively, **["the first and second data paths may be arranged to provide input/output of data burst to or form the cache memory independently of each other" (Col. 2, lines 54-61)]**

wherein in case of sole addressing and accessing the data the access controllers provide access to the memory areas by control ports and address ports of one of the terminals and provides the data through data ports of both terminals **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B" (Col. 5, lines 51-**

62) "data pins 18 and 20 for supporting the output of the 16-bit data signals DQA and DQB for ports A and B" (Col. 6, lines 32-54) "A and B enables a user to combine them into a single 32-bit port. A unified-port mode of operation may be defined by a pre-set control signal supplied via an external pin... in the unified-port mode of operation, an external memory controller provides joint control of corresponding external control and address signals supplied to port A and port B control circuits 22 and 24 so as to perform a single 32-bit write or read access to the SRAM 16 via the both ports... further, if one port of the MPRAM 10 is disabled, the MPRAM 10 would be fully functional via the other port. In particular, any one of ports A and B enables read and write accesses to each and every location in the SRAM 16" (Col. 7, lines 33-56)].

8. As per **claim 28** (new), Camacho discloses the memory unit of claim 24, wherein the first and/or second terminal comprises control ports for receiving control signals for controlling access to the memory areas **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B;" control ports "SCA" and "SCB" (Col. 5, lines 51-62; Figure 1 and related text)].**

9. As per **claim 29** (new), Camacho discloses the memory unit of claim 24, wherein the first and/or second terminal comprises address ports for receiving addressing signals for addressing data within the memory areas **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B;" address ports "ADA" and "ADB" (Col. 5, lines 51-62; Figure 1 and related text)].**

10. As per **claim 30** (new), Camacho discloses the memory unit of claim 29, wherein the address ports provide access to an external address bus **["each of the ports A and B have address and control pins for receiving external address and control signals. The address and control signals for port A are independent from the address and control signals for port B" (Col. 5, lines 51-62; Figure 1 and related text)]**.

11. As per **claim 31** (new), Camacho discloses the memory unit of claim 24, wherein the first and/or second terminal comprises data ports for reading and/or writing data to and/or from the memory areas **["data pins 18 and 20 for supporting the output of the 16-bit data signals DQA and DQB for ports A and B" (Col. 6, lines 32-54; Figure 1 and related text)]**.

12. A per **claims 32-33** (new), Camacho discloses the memory unit of claim 24, wherein the access controllers provide access to the data areas based on control and/or address signals at said terminals wherein the access controllers are state machines, the state machines providing access to the data areas based on states of signals at the first and second terminals. **["SRAM control signals SCA and SCB for the ports A and B, respectively, are supplied via a port A control circuit 22 and a port B control circuit 24 to define SRAM operations such as data read or write, and burst termination" (Col. 3, lines 47-56) "each of the ports A and B comprises a pipelined data path having pipeline stage 1 and pipeline stage 2. The pipeline stages 1 include decoding circuits 110A and 110B, address latches 112A and 112B, and main amplifiers 114A and 114B for ports A and B, respectively... a deselect signal may be supplied to each of the decoding circuits 110A and 110B to inhibit the ports from accepting commands. For example, the deselect signal may be produced when the chip select signal /SS is set to a predetermined state" (Col. 6, lines 15-41; Figure 4 and related text)]**.

13. As per **claim 34** (new), Camacho discloses the memory unit of claim 24, wherein the access controllers comprise memory registers **["write per bit mask registers 34 and 36" (Col. 4, lines 34-51) "data transfer registers 44" (Col. 5, lines 6-21) "mode register" (Col. 5, lines 22-37)]**.

14. As per **claims 35-36** (new), Camacho discloses the memory unit of claim 24, wherein the access controllers provide access to at least one memory area by the control ports and the address ports of the terminals, respectively, and provides the data through the data ports of the terminals, respectively, in case of individual addressing wherein the access controllers provide access to at least one memory area by both of the control ports and the address ports of the terminals, and provide the data through the data ports of the terminals, respectively, in case of individual addressing **["a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length... one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing... each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)]**.

15. As per **claim 37** (new), Camacho discloses the memory unit of claim 24, wherein at least two memory areas are provided **["a cache SRAM memory and a main DRAM memory arranged on the chip" (Col. 2, lines 10-19; Figure 1 and related text)]**.

16. As per **claim 38** (new), Camacho discloses the memory unit of claim 24, wherein programming the size of the memory areas is provided through one of the terminals **["each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 8, lines 27-31)]**.

17. As per **claim 39** (new), Camacho discloses the memory unit of claim 24, wherein one of the terminals provides accessing the data by a central processing unit, and wherein one of the terminals provides accessing the data by a graphics processor **["a multi-port RAM that allows read and write accesses from different ports to be performed simultaneously" (Col. 1, lines 65-67; Col. 1, lines 13-60)]**.

18. As per **claim 40** (new), Camacho discloses the memory unit of claim 24, wherein the bandwidth and/or clocking frequency for the terminals is different **["Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length" (Col. 7, line 57-Col. 8, line 31)]**.

19. As per **claim 43** (new), Camacho discloses a module for providing memory to processors, comprising connection terminals providing communication between an electronic circuit and a memory unit according to claim 24 **[busses (Figure 1 and related text)]**.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. **Claims 25-27** are rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (US 6,167,487) in view of Phelan et al. (US 6,499,089).

22. As per **claim 25** (new), Camacho discloses the memory unit of claim 24, wherein a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively [**"a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length... one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing... each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)**] but does not explicitly disclose the details wherein three memory areas are provided.

Phelan discloses wherein a third memory area a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the

data ports of both of the terminals, respectively as **["multiple array memory device in a single die and, more particularly, to a dual SRAM in a single with configurable sizes" (Col. 1, lines 9-12); "a configurable dual port memory device" (Col. 1, line 63-Col. 2, lines 14) "the ports 102 and 104 may each independently access one or more SRAM blocks" (Col. 2, lines 23-34) wherein "the memory block 122 may comprise a plurality of memory sections 250a-250n. The memory sections 250a-250n may be implemented in one example, as equal sized SRAM blocks... the sections 300a-300n may present the signal MLOGa-MLOGn at a number of outputs 140a-140n. The signals MLOGa-MLOGn may be address signals, or any other type of control and/or access signal" (Col. 3, line 37-Col. 4, line 3; Figure 4 and related text)]**.

Camacho et al. (US 6,167,487) and Phelan et al. (US 6,499,089) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory circuit as disclosed by Camacho and further include three/multiple memory sections/SRAM blocks independently configurable and accessible as taught by Phelan.

The motivation for doing so would have been because Phelan discloses include three/multiple memory sections/SRAM blocks independently configurable and accessible is done to **[save space and decrease costs in the implementation of "a multiple array memory device in a single die and, more particularly, to a dual SRAM in a single die with configurable sizes" (Col. 1, lines 9-37)]**.

Therefore, it would have been obvious to combine Phelan et al. (US 6,499,089) with Camacho et al. (US 6,167,487) for the benefit of creating a memory unit to obtain the invention as specified in claim 25.

23. As per **claim 26** (new), the combination of Camacho and Phelan discloses the memory unit of claim 25, wherein two of the three memory areas provide access by the control ports and the address ports of the terminals, respectively, and the data through the data ports of the terminals, respectively **[The same rationale in the rejection to claims 35-36 is herein incorporated]**.

24. As per **claim 27** (new), the combination of Camacho and Phelan discloses the memory unit of claim 25, wherein the access controllers provide prioritized access to the third memory area through one of the terminals **[Camacho discloses this limitation as "chip select signals /SD and /SS provide chip select functions for the DRAM 12 and the SRAM 16, respectively" (Col. 3, lines 62-64) wherein "if one port of the MRAM 10 is disabled, the MRAM 10 would be fully functional via the other port. In particular, any one of ports A and B enables read and write accesses to each and every location in the SRAM 16" (Col. 7, lines 52-56)]**.

25. **Claim 44** is rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (US 6,167,487) as applied to claim 24 above and further in view of below

26. It is noted that Camacho does not disclose a mobile communication device comprising a memory unit according to claim 24. However, the examiner asserts that it would have been obvious to one ordinary skill in the art at the time the invention was made to use the memory as being claimed in claim 24 in a mobile communication device. A recitation directed to the manner

in which a claim is intended to be used does not distinguish the claim from the prior art if prior art has the capability to do so (See MPEP 2114 and Ex Parte Masham, 2 USPQ2d 1647 (1987).

27. **Claim 46** is rejected under 35 U.S.C. 103(a) as being unpatentable over Camacho et al. (US 6,167,487) as applied to claim 44 above and further in view of Phelan et al. (US 6,499,089).

28. As per **claim 46** (new), Camacho discloses the memory unit of claim 44, wherein a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively **["a set mode register command SMR issued by the DRAM control circuit 42 enables the burst length and type to be programmed in an internal mode register. Ports A and B may be programmed individually so as to allow port A to read or write data burst of one length, whereas port B is enabled to read or write data burst of another length... one port may be programmed to support sequential addressing of data bursts, whereas the other port may be programmed to provide interleave addressing... each port has its own independent burst length counter, burst termination logic and memory addressing logic. Therefore, the burst mode operations for port A may be carried out independently of burst mode operations for port B" (Col. 7, line 57-Col. 8, line 31)]** but does not explicitly disclose the details wherein three storage means are provided.

Phelan discloses providing three memory areas in a memory unit wherein a third memory area a memory area provides access by the control ports and the address ports of both of the terminals, respectively, and the data through the data ports of both of the terminals, respectively as **["multiple array memory device in a single die and, more particularly, to a dual SRAM in a single with configurable sizes" (Col. 1, lines 9-12); "a configurable dual port memory**

device" (Col. 1, line 63-Col. 2, lines 14) "the ports 102 and 104 may each independently access one or more SRAM blocks" (Col. 2, lines 23-34) wherein "the memory block 122 may comprise a plurality of memory sections 250a-250n. The memory sections 250a-250n may be implemented in one example, as equal sized SRAM blocks... the sections 300a-300n may present the signal MLOGa-MLOGn at a number of outputs 140a-140n. The signals MLOGa-MLOGn may be address signals, or any other type of control and/or access signal" (Col. 3, line 37-Col. 4, line 3; Figure 4 and related text)].

Camacho et al. (US 6,167,487) and Phelan et al. (US 6,499,089) are analogous art because they are from the same field of endeavor of computer memory access and control.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify the memory circuit as disclosed by Camacho and further include three/multiple memory sections/SRAM blocks independently configurable and accessible as taught by Phelan.

The motivation for doing so would have been because Phelan discloses include three/multiple memory sections/SRAM blocks independently configurable and accessible is done to **[save space and decrease costs in the implementation of "a multiple array memory device in a single die and, more particularly, to a dual SRAM in a single die with configurable sizes" (Col. 1, lines 9-37)]**.

Therefore, it would have been obvious to combine Phelan et al. (US 6,499,089) with Camacho et al. (US 6,167,487) for the benefit of creating a memory unit to obtain the invention as specified in claim 46.

III. ACKNOWLEDGMENT OF ISSUES RAISED BY THE APPLICANT

Response to Amendment

29. Applicant's arguments filed October 16, 2006 have been fully but are moot in view of new grounds of rejection.

IV. CLOSING COMMENTS

Conclusion

30. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

31. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

V. STATUS OF CLAIMS IN THE APPLICATION

32. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. § 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

33. Per the instant office action, **23-46** have received an action on the merits and are subject of a final rejection.

a(2) CLAIMS NO LONGER IN THE APPLICATION

34. **Claims 1-23** were cancelled by the amendment dated October 16, 2006.

35. For at least the above reasons it is the examiner's position that the applicant's claims are not in condition for allowance.

VI. DIRECTION OF ALL FUTURE REMARKS

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Yaima Campos whose telephone number is (571) 272-1232. The examiner can normally be reached on Monday to Friday 8:30 AM to 5:00 PM.

IMPORTANT NOTE

37. If attempts to reach the above noted Examiner by telephone are unsuccessful, the Examiner's supervisor, Mr. Sanjiv Shah, can be reached at the following telephone number: Area Code (571) 272-4098.

38. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions

on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

December 20, 2006

Yaima Campos
Examiner
Art Unit 2185

SANJIV SHAH
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